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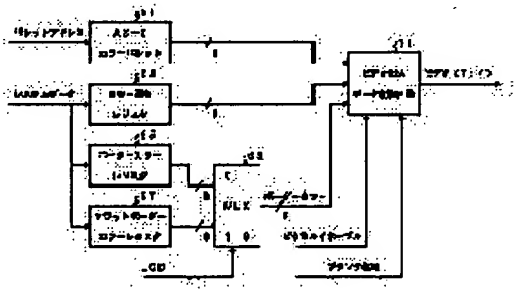
(54) DISPLAY CONTROLLER OF FLAT PANEL DISPLAY

(57)Abstract:

PURPOSE: To provide a display controller of a flat panel display of an STN system or TFT system, etc., having circuits for displaying border colors in the non-display period of this flat panel display.

CONSTITUTION: This display controller has a color pallet 61 and color selection register 63 which color data in order to display the flat boarder colors for coloring the non-display period corresponding to the border colors of a CRT at the time of displaying on the flat panel display, a border color register 65 which is used at the time of displaying the data on the CRT and the flat panel operating at the timing of the CRT interface, a flat border color register 67 which colors the blank period of the flat panel display, a selector which selects two kinds of the colors by the panels, a selector which selects the color selected by the selector, the display period data and the blank data ('0') by a pixel enable signal and a border color enable signal and an OR circuit and AND circuit for forming the border color enable signal by a pixel enable and blank signal and panel type.



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CLAIMS

[Claim(s)]
[Claim 1] A storage means to memorize the border color data displayed on the non-display period of a flat-panel display; The data displayed on the display period of said flat-panel display, It has a means to generate a selection signal for a selection means to choose the border color data memorized by said storage means,;, and said selection means to choose said border color data as said non-display period. The display control characterized by displaying the border color data memorized by said storage means at the non-display period of said flat-panel display.
[Claim 2] As a 2nd storage means to memorize the border color data displayed on the non-display period of a 1st storage means to memorize the border color data displayed on the non-display period of a CRT display, and; flat-panel display, and a; display The signal which shows whether a CRT display is used or a flat-panel display is used is answered. A 1st selection means to choose the border color data memorized by said 1st storage means or the 2nd storage means; The data displayed on the display period of said CRT display or a flat-panel display, A 2nd selection means to choose either of the border color data chosen by said 1st selection means,;, and said 2nd selection means at said non-display period with said 1st selection means The display control characterized by having a means to generate the selection signal for choosing selected border color data.
[Claim 3] Display on the border color period of a 1st storage means to memorize the 1st border color data displayed on the border color period of a CRT display, or the non-display period of a flat-panel display, and; CRT display, or the non-display period of a flat-panel display. A 2nd storage means to memorize the different 2nd border color data from said 1st border color data; The 3rd storage means and; which memorize the selection signal for choosing any shall be used between said 1st border color data and the 2nd border color data A 1st selection means to answer the selection signal memorized by said 3rd storage means, and to choose the 1st or 2nd border color data; The data displayed on the display period of said CRT display or a flat-panel display, A 2nd selection means to choose either of the border color data chosen by said 1st selection means,;, and said 2nd selection means The display control characterized by having a means to generate the selection signal for choosing the border color data chosen as said non-display period by said 1st selection means.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the display control which displays a border color on the non-display period of a flat-panel display about the display control of a flat-panel display.
[0002]
[Description of the Prior Art] The display timing of a CRT display consists of three, a display period, a border color period, and a blanking period, as shown in drawing 11 R> 1. As shown in the level display timing signal of drawing 11 , a display period expires, and a border color signal is displayed until a blanking period starts.
[0003] Drawing 12 shows the example which displayed data in the mode of 400 lines to the with a STN color [of 480 lines / LCD] (only referred to as LCD below) panel. In the example of drawing 12 , the blank period of each upper and lower sides of every 40 lines is established, and a center indication of the data is given. Thus, in the case of LCD, there is no period of a border color, and it consists of a blank period except [all] a display period.
[0004] Drawing 13 is the block diagram of the circuit which performs change control of an indicative data with a display enable signal and a blanking signal. In drawing 13 , the video outlet data control circuit 104 outputs the 8-bit video data which answered the pixel enable signal and doubled the output of a color palette 101, the bit 3 of the color selection register 103, and the bit 2, and outputs the color which answered the blank signal and was set as the border color register 105.
[0005] Drawing 14 is the detail circuit diagram of the video outlet data control circuit of drawing 13 . In the case of CRT, the period of "1" (under a display) is chosen, a selector 107 chooses a color palette output and a color selection register value, and pixel enabling (display enable signal) outputs as an indicative data through the AND gate 109 and the OR gate 111. When the border enable signal outputted from the AND gate 115 is "1", a border color period (period from the end of a display period to the beginning of a blank period) is expressed. That is, the border enable signal whose FLT signal a pixel enable signal is not "1" (not being a display period), and a blank signal is not "1" (not being a blank period), and is not "1" (at the time [An indicating equipment is not a flat-panel display. namely,] of CRT) is set to "1." A border enable signal chooses a border color and outputs the period of "1", and a selector 107 as a video data through the AND gate 113 and the OR gate 11. When a blank signal is "1", a blank period is expressed, this period chooses no selectors 107, but "0" (blank) is outputted as a video outlet.
[0006] In the case of a flat-panel display, as for the period of "1", a selector 107 chooses a color palette output and a color selection register value like [a pixel enable signal] CRT. On the other hand, since a FLT signal is "1" when a flat-panel display is chosen, the output (output of a border enable signal) of the AND gate 115 is "0", and the output of the AND gate 113 is also set to "0." Therefore, when a pixel enable signal is "0", it becomes the same semantics as a blank period. That is, since the output from the AND gate 109 is set to "0" and the output of the AND gate 113 is also set to "0", a selector 107 outputs "0" as a video signal. This period is equivalent to the blank period shown in drawing 11 .

[0007]
[Problem(s) to be Solved by the Invention] Conventionally, since there is no function which displays colors, such as a border color, and "0" data (black) had always come out in addition to the viewing area, in a border color display, there was a problem of being unable to take transposition with a CRT display in flat-panel displays, such as a STN (Single Twisted Nematic) method and a TFT (Thin Film Transistor) method. The purpose of this invention is offering the display control of the flat-panel display equipped with the circuit which displays a border color on the non-display period of flat-panel displays, such as a STN method and a TFT method.
[0008]
[Means for Solving the Problem and its Function] When displaying on a flat-panel display, in order that this invention may display the flat border color which stains the non-display period equivalent to the border color of CRT, The color palette and color selection register which stain at data, The border color register used when displaying data on the flat panel which operates to CRT and CRT interface timing, The flat border color register which stains the blank period of a flat-panel display, The selector which chooses two kinds of colors according to a panel, and the color chosen by the selector, Display period data and the selector which chooses blank data ("0") with a pixel enable signal and a border color enable signal, It has an OR circuit and an AND circuit for pixel enabling, a blank signal, and a panel type to generate a border color enable signal.
[0009]
[Example] Hereafter, the example of this invention is explained with reference to a drawing. First, with reference to drawing 1 , the configuration of whole Display Control System which used the display controller concerning one example of this invention is explained. This Display Control System 4 is Display Control System of a VGA (Video Graphics Array) specification with display modes, such as for example, a 640x480-dot 256 color coincidence display, and is connected to the system bus 2 of a portable computer through the bus connector 3. This Display Control System 4 performs the display control to the flat-panel display 40 and color CRT display 50 both sides to which option connection is made with which the body of a portable computer is equipped standardly.
[0010] The display controller 10 and the image memory 25 are established in Display Control System 4. These display controllers and an image memory 25 are carried on the circuit board which is not illustrated.
[0011] A display controller 10 is LSI realized by the gate array, and accomplishes the principal part of this Display Control System 4. It is combined with CPU1 of a portable computer through the bus connector 3 and the system bus 2, and this display controller 10 performs drawing to an image memory 25 according to the demand from CPU1. Moreover, a display controller 10 changes into a video data the data drawn by the image memory 25, outputs to a flat-panel display 40 or the color CRT display 50, and performs those screen refreshes.
[0012] An image memory (VRAM) 25 memorizes the indicative data for displaying on a flat-panel display 40 or the color CRT display 50, and consists of two DRAM chips. Four maps (MAP0-MAP3) are defined as this image memory 25, MAP0 and MAP1 are realized by one DRAM, and MAP2 and MAP3 are realized by DRAM of another side.
[0013] An image memory 25 has data input/output port of the 32-bit width of face corresponding to the memory data MD 31-0. In this case, in the memory data [MAP / MD and / 1] 7-0, MD 15-8 and MAP2 correspond to MD 23-16, and MAP3 corresponds [MAP0] to MD 31-24. Moreover, addressing of these [MAP0-MAP3] is carried out in common by the memory address (MA 9-0).
[0014] The memory control signal (row address strobe signal RAS, the column-address strobe signal CAS, the write enable signal WE, output enable signal OE) is prepared two kinds, and it is used by BRAS, BCAS, and BWE and BOE by being used as a control signal of DRAM as a control signal of DRAM of another side where MAP2 and MAP3 are realized while, as for ARAS, ACAS, and AWE and AOE, MAP0 and MAP1 are realized.
[0015] In graphics mode, graphics data are drawn by the image memory 25 with a memory plane method. This memory plane method is a method which uses all (MAP0-MAP3) of four maps, and

assigns the color information on each pixel to these maps. In this case, 1 pixel is expressed for every map by total (4 bits per pixel) of every 1 bit data [4-bit]. Since the data input/output port of an image memory 25 is 32-bit width of face, the graphics data of 4 bits per pixel are read by 8 dots by one read access.

[0016] Moreover, in a text mode, a character code, an attribute, and alphabetic character font data are stored in an image memory 25. In a text mode, three of four maps (MAP0-MAP3) defined as the image memory 25 (MAP0-MAP2) are used. The character code for one screen for a display is stored in MAP0, and the attribute for one screen corresponding to it is stored in MAP1. The text data for one character has the data size of a total of 2 bytes which consists of a 8 bits character code and a 8-bit attribute. 8-bit attribute data contain 4 bit data (bit4-bit7) which specify the color (background color) of the 4 bit data (bit0-bit3) and the background which specify the color (alphabetic character color) of a foreground. The data of bit3 are used also for selection of an alphabetic character kind, or high brightness assignment of an alphabetic character color among 4 bit data (bit0-bit3) which specify the color (alphabetic character color) of a foreground.

[0017] Moreover, eight kinds of font sets are stored in MAP2. Each font set contains the selectable alphabetic character font data for 256 characters by the 8-bit character code. Each alphabetic character font data has the data size corresponding to font patterns, such as 8 dot x16 line or 9 dot x16 line.

[0018] The display controller 10 consists of a clock synthesizer 11, the CRT control circuit 12, the CPU interface 13, the display address-generation circuit 14, the raster operation circuit 15, attribute control and the parallel/serial-conversion circuit (P/S) 16, the memory control circuit 17, a color palette 18, RAMDAC19, a flat panel emulation circuit 20, a clock selector 21, and a power down control circuit 22 like illustration. All the circuits except this display controller's 10 memory control circuit 17 operate to the timing which synchronized with the video clock VDLK. Hereafter, the function of each circuit is explained.

[0019] A clock synthesizer 11 generates the video clock VDCLK, the memory clock MCLK, the character clock CRCK, etc. based on the system clock SYSCLK from a system bus 2.

[0020] The video clock VDCLK is a synchronous clock for outputting a video signal to these displays per dot according to the display timing of a flat-panel display 40 or CRT display 50, for example, has the frequency of about 28.322MHz. The value of the frequency of this video clock VDCLK is determined based on the horizontal/vertical scan frequency of a flat-panel display 40 or CRT display 50.

[0021] The memory clock MCLK is a clock of the memory control circuit 17 of operation, can specify the frequency only with the engine performance of an image memory 25, for example, has a value higher than the video clock VDCLK of 41.612MHz.

[0022] The character clock CRCK is a clock outputted per one character, for example, when the longitudinal direction size of the font data of one character is 9 dots, the character clock CRCK has the clock VDCLK 9 times the period of video.

[0023] Two or more PLL circuits for generating various clocks are built in this clock synthesizer 11. The power down signal PD from the power down control circuit 22 is supplied to the PLL circuit used for generation of the video clock VDCLK. This power down signal PD is for carrying out power down of the PLL circuit which generates the video clock VDCLK.

[0024] The display timing control circuit 12 controls the display timing of flat panel DIPUREI 40 and CRT display 50. That is, the display timing control circuit 12 generates the various control signals (Horizontal Synchronizing signal HSYNC, Vertical Synchronizing signal VSYNC) for controlling the various control signals (the Rhine pulse LP, the field pulse FP, and shift clock SCK) for controlling the display timing of flat panel DIPUREI 40, and the display timing of CRT display 50 based on the timing information set as the video clock VDCLK, the character clock CRCK, and a parameter register group from the clock synthesizer 11. The shift clock SCK to flat panel DIPUREI 40 is used as a data shift signal for shifting and incorporating a video data in a flat-panel display 40.

[0025] Moreover, the display timing control circuit 12 supplies the display address to the display address-generation circuit 14 while supplying a display initiation timing signal to the memory control

circuit 17. Furthermore, the display timing control circuit 12 publishes the interrupt request signal (IRQ) over CPU1.

[0026] The CPU interface 13 is for delivering and receiving system data D15-0 grade with CPU1 through a system bus 2, and the parameter register group is prepared in this CPU interface 13. A parameter register group holds the display mode (a text mode, graphics mode) of flat panel DIPUREI 40 and CRT display 50, and the various parameters for specifying display timing etc. This parameter is given from CPU1 through system data D 15-0. The read/write of a parameter to a parameter register is controlled by the I/O lead signal IOR and the IO light signal IOW.

[0027] Moreover, the CPU interface 13 outputs MEMCS16 signal and IOCS16 signal while inputting a SBHE signal from a system bus 2. A SBHE signal shows a transfer of high-order byte D 15-8 of system data D 15-0. MEMCS16 signal and IOCS16 signal are outputted at the time of activation of a 16-bit memory cycle and a 16-bit I/O cycle, respectively.

[0028] Furthermore, the CPU interface 13 outputs the mode recognition signal (a text/graph) with which the display mode specified by CPU1 shows a text mode (T) and graphics mode (G). This mode recognition signal is set to "1" when the parameter which shows "0" and a text mode when the parameter which shows graphics mode to the predetermined register of a parameter register group is set is set. A mode recognition signal is supplied to the memory control circuit 17 and the clock selector 21, and power down control circuit 22 grade.

[0029] The display address-generation circuit 14 generates the memory address MA 9-0 for carrying out read/write access of the image memory 25 according to the system address SA 19-0 from CPU1, or the display address from the CRT control circuit 12. In this case, a memory address MA 9-0 consists of a row address of 10-bit width of face, and a column address of 10-bit width of face, and these row addresses and a column address are given to an image memory 25 from the display address-generation circuit 14 by time sharing.

[0030] Moreover, the AEN signal inputted into the display address-generation circuit 14 from a system bus 2 shows effective/invalid of the system address SA 19-0. The raster operation circuit 15 has the function transmitted to the memory control circuit 17 by CPU1 by using as light data the system data D 15-0 set to the parameter register group, and the drawing function which performs various raster operations to the indicative data read from the image memory 25 by the memory control circuit 17. At the time of drawing, logical operation is performed by the raster operation circuit 15, and, as for the indicative data read from the image memory 25, the result of an operation is again written in an image memory 25. The contents of the operation are controlled by the parameter set as the parameter register group. Moreover, the drawing data from CPU1 carry out through [of the CPU interface 13 and the raster operation circuit 15], and are transmitted to the memory control circuit 17.

[0031] Attribute control and the parallel/serial-conversion circuit (P/S) 16 generate the data for inputting into a color palette 18. In graphics mode, after the 32 bits (8 pixels) graphics data read from MAP0-MAP3 of an image memory 25 at once are cut down one by one by attribute control and the parallel/serial-conversion circuit (P/S) 16 per 1 pixel of 4 bits per pixel, it is inputted into a color palette 18. On the other hand, in a text mode, first, 8 dots of the font data corresponding to a certain character code are read from MAP2 of an image memory 25 at once, and it is started by parallel/serial conversion per 1 dot. Then, according to the value of the font of that started 1-dot unit, one side of the 4 bits foreground of attribute data and a 4-bit background is chosen, and those 4 selected bit data are inputted into a color palette 18.

[0032] The memory control circuit 17 carries out the access control of the image memory 25 according to the memory read/write demand (MEMR, MEMW) from the timing or CPU1 of screen refresh. This memory control circuit 17 is the timing which synchronized with the input clock CLK, and generates the write enable signal AWE MAP0 and for MAP1, the output enable signal AOE, row address strobe signal ARAS, the column-address strobe signals MAP [ACAS and] 2 and the write enable signal BWE for MAP3, the output enable signal BOE, row address strobe signal BRAS, and the column-address strobe signal BCAS.

[0033] When performing screen refresh, the memory control circuit 17 starts the read access of an image

memory 25 by making the display initiation timing signal from the CRT control circuit 12 into a trigger.
[0034] When a mode recognition signal shows graphics mode, the memory control circuit 17 carries out the serial access of the image memory 25 by the fast page mode read cycle. Once the graphics data read by this serial access are held at the FIFO buffer which is not illustrated in the memory control circuit 17, they are transmitted to attribute control and the parallel/serial-conversion circuit 16.
[0035] On the other hand, when a mode recognition signal shows a text mode, the memory control circuit 17 carries out random access of the image memory 25 by the single read cycle. The text data read by random access is directly transmitted to attribute control and the parallel/serial-conversion circuit 16, without minding FIFO buffers 171a and 171b.
[0036] Moreover, the memory control circuit 17 controls the Arbitration of screen refresh and drawing processing of CPU1. When the memory read/write demand (MEMR, MEMW) from the read access and CPU1 for screen refresh competes, the memory control circuit 17 generates an I/O-channel ready signal (IOCHRDY), and extends the bus cycle of CPU1.
[0037] The color palette control circuit 18 is for determining the color attribute of the data of 4 bits per pixel outputted from attribute control and the parallel/serial-conversion circuit (P/S) 16, and is equipped with the color palette table containing 16 color palette registers. The data of 4 bits per pixel from attribute control and the parallel/serial-conversion circuit (P/S) 16 are inputted into this color palette table as an index, and one of the 16 color palette registers is chosen as it. 6-bit color palette data are set to each color palette register. 2 bits outputted from the color selection register of color palette control circuit 18 built-in are added to the 6-bit color palette data read from the selected color palette register, and the data which are 8 bits in total are outputted to them. These 8 bit data are supplied to RAMDAC19 as a CRT video data.
[0038] RAMDAC19 consists of D/A converters which change into an analog signal the color data read from the color table which it is and makes a 8-bit CRT video data the index and this color table for generating the analog color video signal of R, G, and B for color CRT display 50. Since there is a display mode of a 256 color coincidence display by the VGA specification, in order to support this display mode, 256 color registers are contained in the color table, and one of them is chosen by the CRT video data. each color register -- R, G, and B -- a total of the 18-bit color data which consist of 6 bits about each is stored. The color data stored in the selected color register are supplied to the D/A converter of RAMDAC19 built-in while they are supplied to the flat panel emulation circuit 20 as digital one R, G, and B data. A D/A converter changes digital one R, G, and B data into Analogs R and G and B signal, and supplies them to CRT display 50.
[0039] the flat panel emulation circuit 20 -- digital one -- R, G, and B data are emulated to the color or gray shade video data for flat-panel display 40.
[0040] The clock selector 21 chooses one side of the memory clock MCLK and the video clock VDCLK as an input clock CLK of the memory control circuit 17. In this case, selection actuation of the clock selector 21 is controlled by the mode recognition signal from the CPU interface 13. Namely, the video clock VDCLK is chosen at the time of "0" "1" memory clock MCLK is chosen at time of level, and mode recognition signal indicates text mode to be level a mode recognition signal indicates graphics mode to be.
[0041] When the power down control circuit 22 detects the change to a text mode from graphics mode with a mode recognition signal, it generates the power down signal PD. This power down signal PD carries out the disable of the PLL for memory clock MCLK generating in a clock synthesizer 11, and carries out power down of it. Moreover, when the power down control circuit 22 detects the change in graphics mode from a text mode with a mode recognition signal, in order to enable PLL for memory clock MCLK generating, it suspends generating of the power down signal PD. Furthermore, the power down control circuit 22 also performs power down control of RAMDAC19. Disable control for power down can be performed by the technique of intercepting the current supply to the circuit, and supply of a clock of operation, for example.
[0042] Drawing 2 is the block diagram of the video outlet data control circuit in the example of the display control of this invention, and its periphery. In drawing 2 , a color palette 61, a multiplexer 69,

and the video outlet data control circuit 71 are formed in the color palette 18 shown in drawing 1 , and the color selection register 63, the border color register 65, and the flat border color register 67 are a part of parameter register groups in CPUI/F13 of drawing 1 .

[0043] A color palette 61 outputs 6 bits of low order of a video data (address of the color look-up table in RAMDAC19). The color selection register 63 outputs 2 bits of high orders of a video data. The 6-bit output of a color palette 61 and the 2-bit output of the color selection register 63 are supplied to the video-data output-control circuit 71. The border color register 65 holds the border color in a border color period, when using CRT. The flat baud DARA register 67 holds the color in a blanking period, when using the LCD panel. The 8-bit output of the border color register 65 and the 8-bit output of the flat border color register 67 are supplied to a multiplexer 69. A multiplexer 69 changes the value of the border color register 65, and the value of the flat border color register 67 according to the class of indicating equipment, and supplies them to the video outlet data control circuit 71 as a border color signal. In this example, a multiplexer 69 chooses the value of border color REJISUA 69, when a LCD signal (set to "1" when an indicating equipment is a flat panel (LCD)) is "0", and when a LCD signal is "1", it chooses the value of the flat border color register 67. The video outlet data control circuit 71 chooses an indicative data and a border color with a pixel enable signal and a blank signal. That is, when a pixel enable signal is "1", 6 bits from a color palette 61 and 2 bits a total of 8 bits from the color selection register 63 are outputted as a video data, and when a blank signal is "1", the border color from a multiplexer 69 is outputted as a video data.

[0044] Drawing 3 is the detail circuit diagram of the video outlet data control circuit 71 shown in drawing 2 . The AND gate 75 in a selector 73 outputs 6 bits from a color palette 61, and 2 bits a total of 8 bits from the color selection register 63 as a video data through the OR gate 79, when a pixel enable signal is "1" (when it is a display period), and the AND gate 77 outputs the border color from the border color register 65 or the flat border color register 67 as a video data through the OR gate 79, when a border enable signal is "1."

[0045] the OR gate 83 and the AND gate 81 -- a pixel enable signal -- "1" -- not but (a display period -- not but) -- and a pixel enable signal when a blank signal is not "1" (it is not a blank period) -- "1" -- not but (a display period -- not but) -- and when a LCD signal is "1", the border enable signal of "1" is outputted to a selector 73 (when an indicating equipment is LCD).

[0046] Actuation of one example of this invention constituted as mentioned above is explained. If the system shown in drawing 1 starts, a default will be set to each of a color palette 61, the color selection register 63, the border color register 65, and the flat border color register 67 by System BIOS.

[0047] (i) When LCD is chosen as a display, since a LCD signal is "1", the multiplexer 69 of drawing 2 chooses the value of the flat border color register 67 in this case. Moreover, the output of the OR gate 83 of drawing 3 is set to "1" regardless of the value of a blank signal. Therefore, the output of the AND gate 81 is determined by the logical level of a pixel enable signal.

[0048] Initiation of a display repeats a display period and a non-display period, as shown in (b) of the timing chart (vertical display timing) of drawing 4 . If a pixel enable signal is set to "1" and it enters at a display period, in the selector 73 of drawing 3 , the AND gate 75 will output the output of a color palette 61, and the output of the color selection register 63 as a video data through the OR gate 79. In addition, since the output of the AND gate 81 is "0" at this time, a border enable signal is not outputted. Therefore, the AND gate 77 does not output a border color. Next, if a pixel enable signal is set to "0" and it enters at a non-display period, the AND gate 81 will output a border enable signal to the AND gate 77. Consequently, the AND gate 77 outputs a border color (value of the flat border color register 67) through the OR gate 79.

[0049] (ii) When CRT is chosen as a display, since a LCD signal is "0", a multiplexer 69 chooses the value of the border color register 65 as a border color in this case. If a pixel enable signal is set to "1" and it enters at a display period, in the selector 73 of drawing 3 , the AND gate 75 will output the output of a color palette 61, and the output of the color selection register 63 as a video data through the OR gate 79. Next, if a pixel enable signal is set to "0" and a blank signal is set to "0", it will enter at a border color period. In this period, the output of the AND gate 81 is set to "1", and outputs a border enable

signal to the AND gate 77. Consequently, the AND gate 77 outputs a border color (value of the border color register 65) through the OR gate 79. Then, if a blank signal is set to "1", since the output of the OR gate 83 will be set to "0", the AND gate 81 does not output a border enable signal. For this reason, both the outputs of the AND gate 75 and the AND gate 77 are set to "0", and the video data of "0" is outputted.

[0050] The table of truth value which expresses the relation of the LCD signal, the pixel enable signal, blank signal, and video outlet the case of CRT and in the case of LCD to drawing 5 is shown. In addition, it is horizontally the same although the above-mentioned example explained perpendicularly. Moreover, like [in the coincidence display of CRT and LCD], although considered as the configuration which forms the border color register 65 for setting the border color for CRT, and the flat border color register 67 which sets the border color for LCD in the above-mentioned example, when using the same border color color, a border color register can be set to one.

[0051] By the way, the number of display Rhine of application is distinguished with the polarity of the horizontal which a display controller outputs, and a Vertical Synchronizing signal, and the panel which indicates by centering automatically is in the LCD panel. In the case of this panel, only the number range of Rhine of application (the number of display Rhine) can control a display controller to be shown in drawing 6 . For this reason, the way things stand, a border color cannot be displayed on a blank period. Therefore, in order to display a border color by the display controller side, it is necessary to be made not to perform automatic centering by the approach mentioned above. The method of forbidding automatic centering is explained in full detail by the "display control" (application number-H04-138753, filing date of application: May 29, Heisei 4) for which the same applicant applied. (When carrying out a stretch and displaying to the limit of a screen, this patent is changed so that a synchronizing signal polarity may be doubled with the number of Rhine by the side of a panel (this example 480 lines) regardless of application.) In this application, a stretch quotes only the circuit for displaying but to the limit [of the number of Rhine of a panel] independently. Consequently, automatic centering is not performed, but as shown in drawing 7 , a display begins from a screen head. If a display controller carries out the same centering as a flat panel in this condition, it becomes like drawing 8 and a border color can be expressed as the approach mentioned above. Drawing 9 shows the timing chart of Vertical Synchronizing signal FP at the time of performing application which performs the display of 400 lines using the flat panel (the TFT panel which operates to CRT timing in this example) of 640x480 dots, the effective display period signal FVDSP, and a data signal. It is indicated by the "display conversion circuit" (application number-H02-322639, filing date of application: November 28, Heisei 2) about the method of centering.

[0052] Next, the 2nd example of this invention is explained. In addition, the same section as the 1st example shown in drawing 2 attaches a same sign, and omits explanation. It is more convenient to necessarily have not prepared a specified register, respectively and to use the same border color especially in the coincidence display of CRT and a flat panel, although considered as the configuration which forms the border color register 65 for CRT, and the flat border color register 67 for flat panels in the 1st example shown in drawing 2 . In this 2nd example, it has the border register 68 with which the border signal (BORDER) which specifies which border color of the 1st border color register 64 with which the 1st border color is set, the 2nd border color register 66 with which the 2nd border color is set, and the 1st border color and the 2nd border color is chosen is set. While each output of the 1st border color register 64 and the 2nd border color register 66 is supplied to each input of a multiplexer 69, respectively, the output of the border register 68 is supplied to the selection terminal S of a multiplexer 69. When a border signal is "0", at the time of "1", a multiplexer 69 makes the 1st border color a border color signal, and supplies the 2nd border color for it to the video outlet data control circuit 71. Thus, it can be used by constituting, being able to change the border color of two or more colors.

[0053]

[Effect of the Invention] As stated above, though it is a color panel, according to this invention, the same border color as CRT can be displayed on the non-display field of the flat panel which did not indicate by the black deer. For this reason, a border display will be clear and there is effectiveness, like

compatibility with CRT can be taken.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the display control which displays a border color on the non-display period of a flat-panel display about the display control of a flat-panel display.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As stated above, though it is a color panel, according to this invention, the same border color as CRT can be displayed on the non-display field of the flat panel which did not indicate by the black deer. For this reason, a border display will be clear and there is effectiveness, like compatibility with CRT can be taken.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Conventionally, since there is no function which displays colors, such as a border color, and "0" data (black) had always come out in addition to the viewing area, in a border color display, there was a problem of being unable to take transposition with a CRT display in flat-panel displays, such as a STN (Single Twisted Nematic) method and a TFT (Thin Film Transistor) method. The purpose of this invention is offering the display control of the flat-panel display equipped with the circuit which displays a border color on the non-display period of flat-panel displays, such as a STN method and a TFT method.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram of whole Display Control System which used the display control in connection with one example of this invention.
[Drawing 2] The video outlet data control circuit in the display control of this invention, and the block diagram of the circumference of it.
[Drawing 3] The detail circuit diagram of the video-data output-control circuit shown in drawing 2 .
[Drawing 4] The timing chart which shows the display timing of the perpendicular direction of LCD and CRT in the above-mentioned example.
[Drawing 5] Table of truth value showing the relation of the LCD signal, the pixel enable signal, blank signal, and video outlet the case of CRT, and in the case of LCD.
[Drawing 6] The explanatory view showing the range which the display controller is controlling in a flat panel with an automatic centering function.
[Drawing 7] The conceptual diagram showing the display at the time of forbidding centering in the flat panel which has an automatic centering function.
[Drawing 8] The conceptual diagram showing the range which a display controller controls in the flat panel which forbade centering.
[Drawing 9] It is TFT as a flat panel. The Vertical Synchronizing signal at the time of using LCD, an effective display period signal and an indicative data, timing chart that shows each timing of a flat border color display.
[Drawing 10] The block diagram showing the 2nd example of the display control of this invention.
[Drawing 11] The explanatory view showing the display timing of a CRT display.
[Drawing 12] The conceptual diagram showing the example which displayed data in the mode of 400 lines on a with a STN color [of 480 lines / LCD] panel.
[Drawing 13] The block diagram of the conventional video-data output-control circuit.
[Drawing 14] The detail circuit diagram of the video-data output-control circuit shown in drawing 13 .
[Description of Notations]
1 ... CPU and 4 ... Display Control System and 40 ... a flat-panel display and 50 ... a CRT display and 61 ... a color palette and 63 ... a color selection register and 65 ... a border color register and 67 ... a flat border color register and 69 ... a multiplexer and 71 ... a video outlet control circuit and 73 ... a selector, and 75, 77 and 81 ... the AND gate, and 79 and 83 ... the OR gate

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[Translation done.]

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PRIOR ART

[Description of the Prior Art] The display timing of a CRT display consists of three, a display period, a border color period, and a blanking period, as shown in drawing 11 R> 1. As shown in the level display timing signal of drawing 11 , a display period expires, and a border color signal is displayed until a blanking period starts.
[0003] Drawing 12 shows the example which displayed data in the mode of 400 lines to the with a STN color [of 480 lines / LCD] (only referred to as LCD below) panel. In the example of drawing 12 , the blank period of each upper and lower sides of every 40 lines is established, and a center indication of the data is given. Thus, in the case of LCD, there is no period of a border color, and it consists of a blank period except [all] a display period.
[0004] Drawing 13 is the block diagram of the circuit which performs change control of an indicative data with a display enable signal and a blanking signal. In drawing 13 , the video outlet data control circuit 104 outputs the 8-bit video data which answered the pixel enable signal and doubled the output of a color palette 101, the bit 3 of the color selection register 103, and the bit 2, and outputs the color which answered the blank signal and was set as the border color register 105.
[0005] Drawing 14 is the detail circuit diagram of the video outlet data control circuit of drawing 13 . In the case of CRT, the period of "1" (under a display) is chosen, a selector 107 chooses a color palette output and a color selection register value, and pixel enabling (display enable signal) outputs as an indicative data through the AND gate 109 and the OR gate 111. When the border enable signal outputted from the AND gate 115 is "1", a border color period (period from the end of a display period to the beginning of a blank period) is expressed. That is, the border enable signal whose FLT signal a pixel enable signal is not "1" (not being a display period), and a blank signal is not "1" (not being a blank period), and is not "1" (at the time [An indicating equipment is not a flat-panel display. namely,] of CRT) is set to "1." A border enable signal chooses a border color and outputs the period of "1", and a selector 107 as a video data through the AND gate 113 and the OR gate 11. When a blank signal is "1", a blank period is expressed, this period chooses no selectors 107, but "0" (blank) is outputted as a video outlet.
[0006] In the case of a flat-panel display, as for the period of "1", a selector 107 chooses a color palette output and a color selection register value like [a pixel enable signal] CRT. On the other hand, since a FLT signal is "1" when a flat-panel display is chosen, the output (output of a border enable signal) of the AND gate 115 is "0", and the output of the AND gate 113 is also set to "0." Therefore, when a pixel enable signal is "0", it becomes the same semantics as a blank period. That is, since the output from the AND gate 109 is set to "0" and the output of the AND gate 113 is also set to "0", a selector 107 outputs "0" as a video signal. This period is equivalent to the blank period shown in drawing 11 .

[Translation done.]

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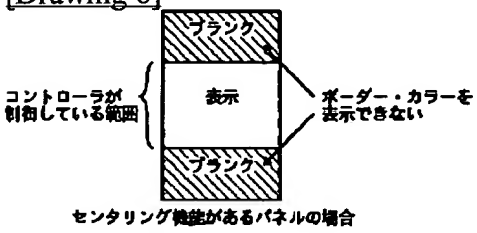
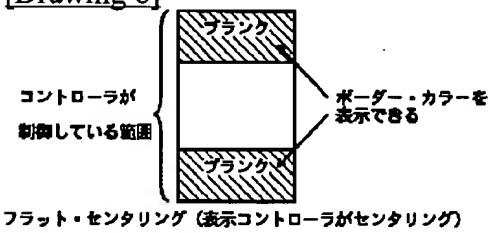
DRAWINGS

[Drawing 6]

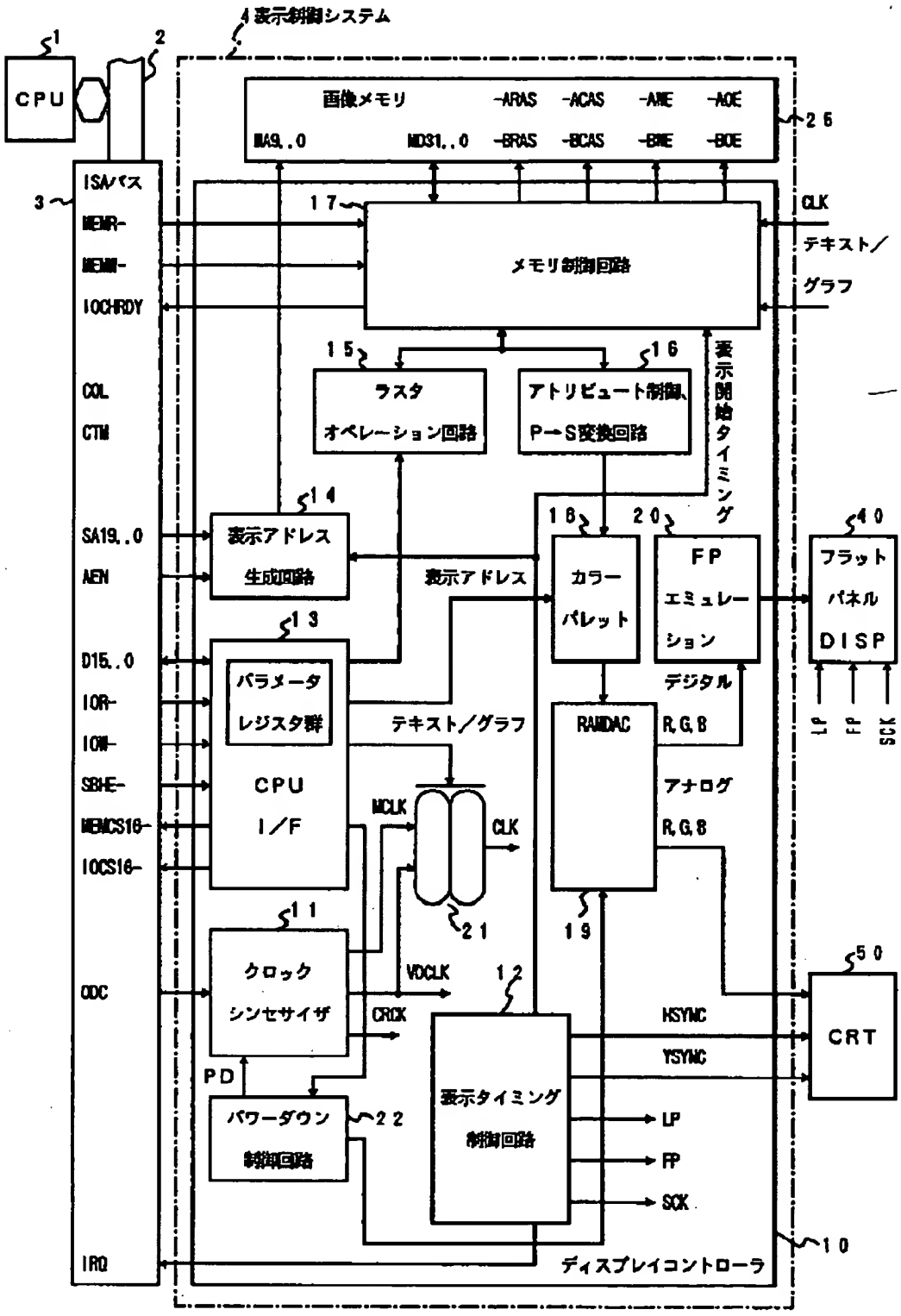


[Drawing 7]

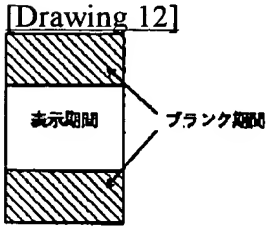
[Drawing 8]



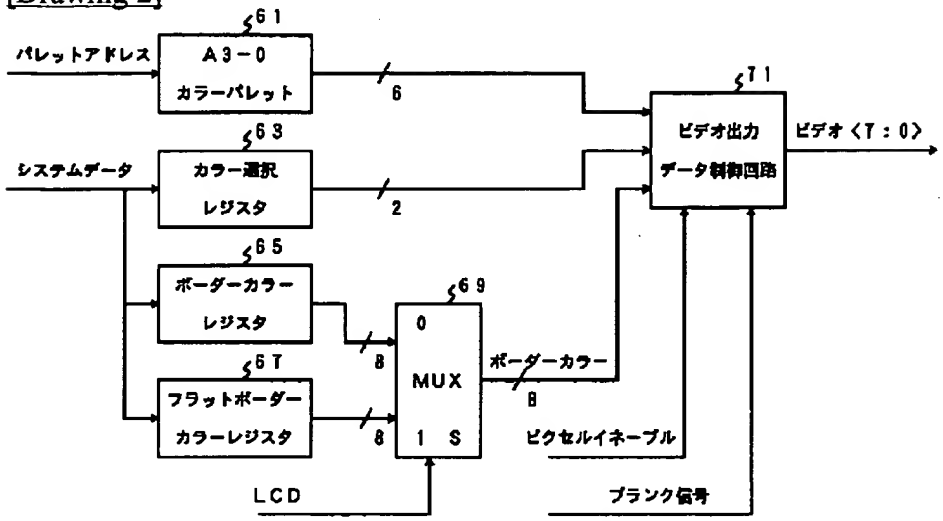
[Drawing 1]


4 表示制御システム
CPU
画像メモリ
-ARAS -ACAS -AWE -AOE
MA9..0 MD31..0 -BRAS -BCAS -BWE -BOE
26
ISAバス
MEMR-
MEMW-
IOCHRDY
17
メモリ制御回路
CLK
テキスト/グラフ
15
ラスタ
オペレーション回路
16
アトリビュート制御、
P→S変換回路
表示開始タイミング
COL
CTM
SA19..0
AEN
14
表示アドレス
生成回路
表示アドレス
18
カラー
パレット
20
FP
エミュレーション
40
フラットパネル
DISP
LP
FP
SCK
D15..0
IOR-
IOW-
SBHE-
MEMCS16-
IOCS16-
13
パラメータ
レジスタ群
CPU
I/F
テキスト/グラフ
デジタル
RAMDAC
R,G,B
アナログ
R,G,B
MCLK
CLK
21
19
11
クロック
シンセサイザ
VOCLK
12
CRCK
HSYNC
YSYNC
50
CRT
PD
パワーダウン
制御回路
22
表示タイミング
制御回路
LP
FP
SCK
IRQ
ディスプレイコントローラ
10

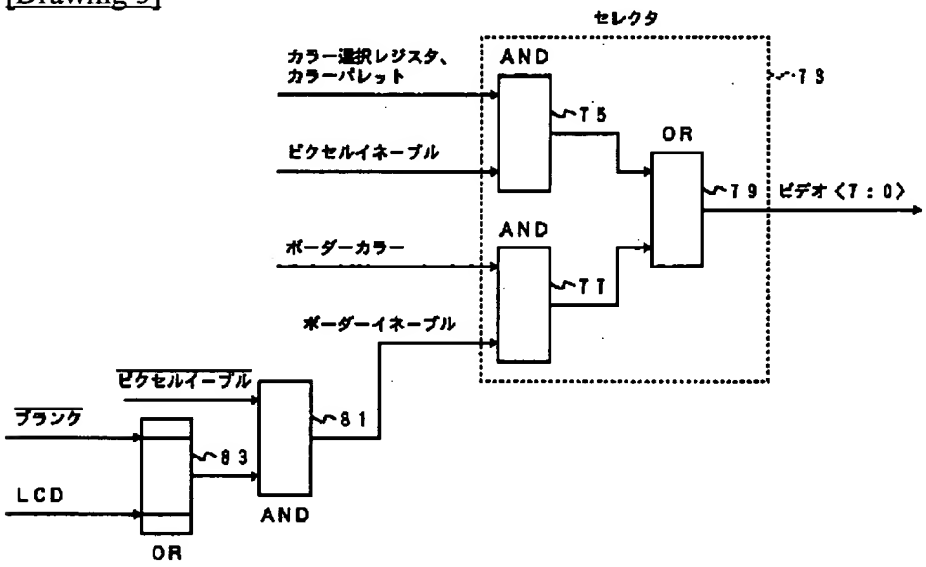
[Drawing 12]


表示期間
ブランク期間

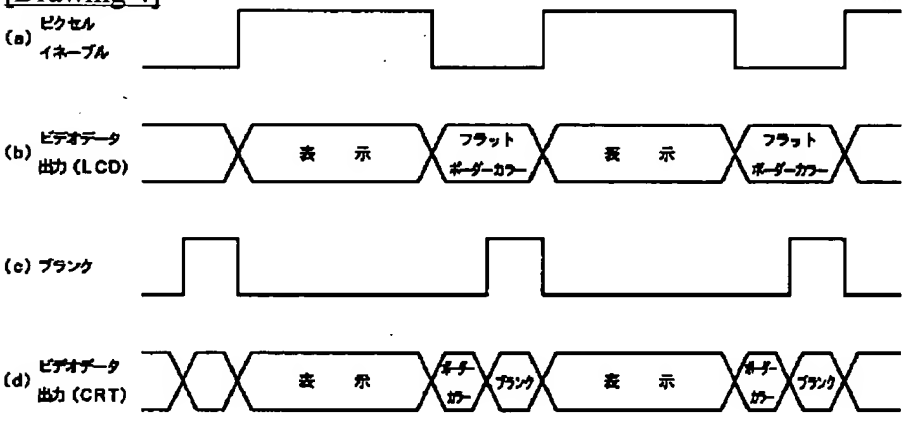
[Drawing 2]



[Drawing 3]



[Drawing 4]

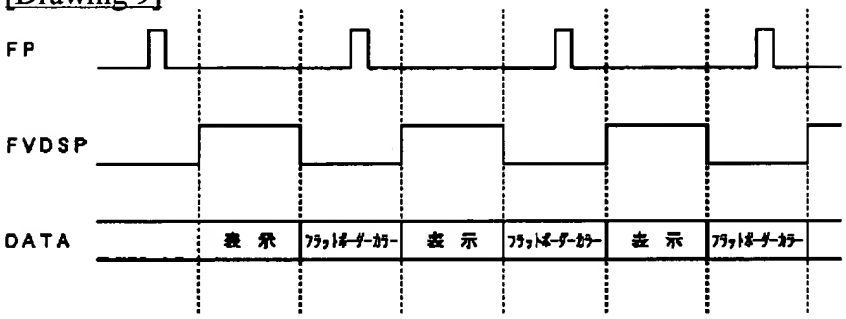


[Drawing 5]

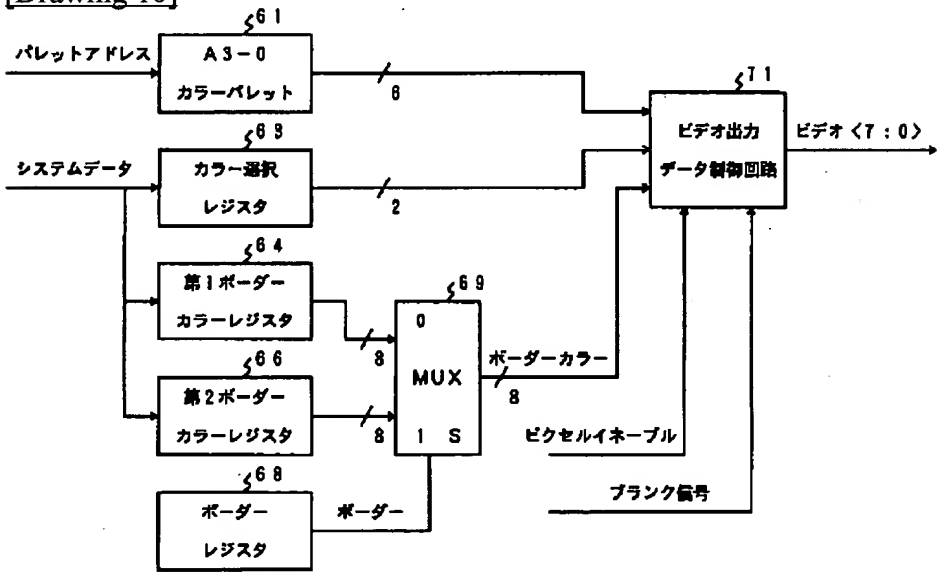
真理値表

	LCD	ピクセルイネーブル	ブランク信号	ビデオ出力
CRT	0	0	0	ボーダー・カラー
CRT	0	0	1	"0"
CRT	0	1	0	カラー選択、カラー・パレット値
LCD	1	0	X	ボーダー・カラー
LCD	1	1	X	カラー選択、カラー・パレット値

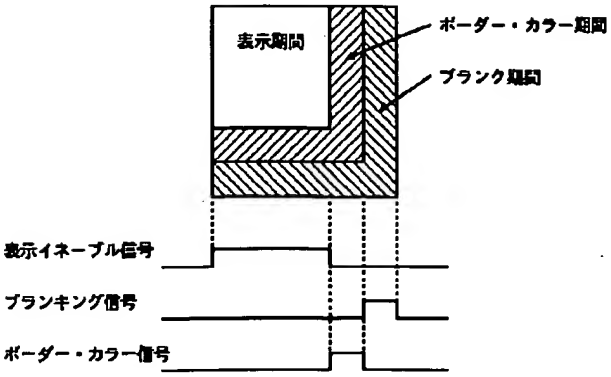
[Drawing 9]



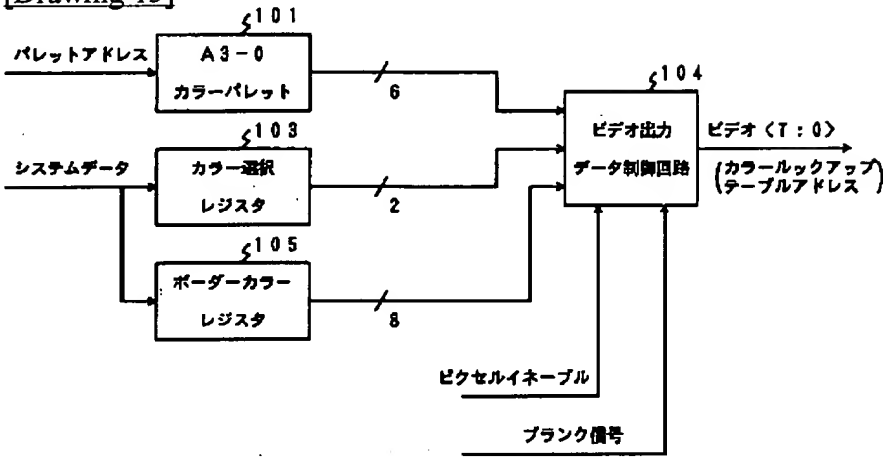
[Drawing 10]



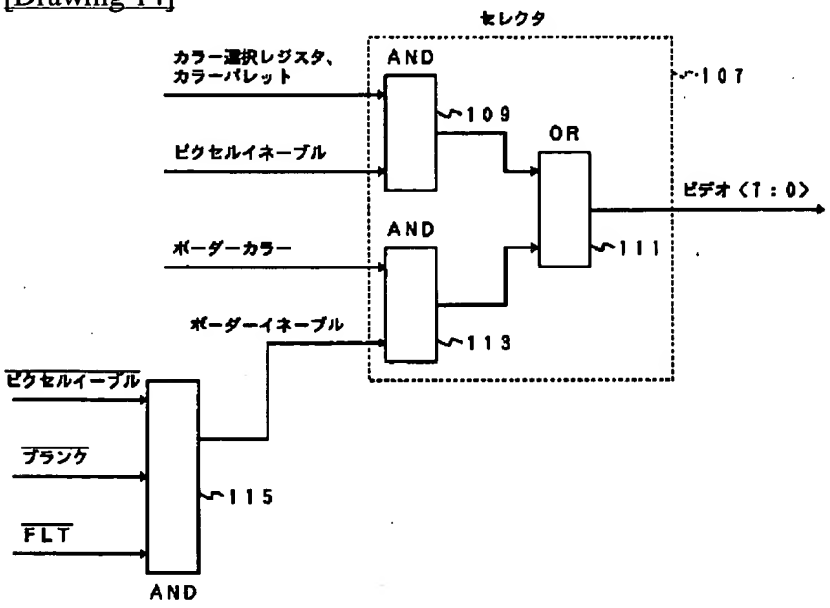
[Drawing 11]



[Drawing 13]



[Drawing 14]



[Translation done.]